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FUR920040031US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Burda, et al.

Serial No.: 10/711079 Group Art Unit: Unknown

Filing Date: 08/20/04 Examiner: Unknown

For: A METHOD AND SYSTEM FOR INTELLIGENT AUTOMATED RETICLE MANAGEMENT

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicants' duty of disclosure under 37 CFR §1.56, applicants respectfully bring the following documents, listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copies of the listed documents are provided herewith for the convenience of the Examiner. This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicants are aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,

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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
BUR920040031US1	10/711079
Applicant(s)	
Burda, et al.	
Filing Date	**Group Art Unit**
08/20/04	Unknown

EXAMINER INITIAL		OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*
		Nadoli, et al, "SIMULATION IN AUTOMATED MATERIAL HANDLING SYSTEMS DESIGN FOR SEMICONDUCTOR MANUFACTURING", Proceedings of the 1994 Winter Simulation Conference, pp. 892-899
		Park, et al., "ASSESSMENT OF POTENTIAL GAINS IN PRODUCTIVITY DUE TO PROACTIVE RETICLE MANAGEMENT USING DISCRETE EVENT SIMULATION", Proceedings of the 1999 Winter Simulation Conference, pp. 856-864
		Campbell, et al., "A MODEL OF A 300MM WAFER FABRICATION LINE", Proceddings of the 1999 Winter Simulation Conference, pp. 909-911
		Lee, et al., "DISPATCHING HEURISTIC FOR WAFER FABRICAITON", Proceedings of the 2001 Winter Simulation Conference, pp. 1215-1219
		White, Jr., et al., "OPERATIONAL SIMULATION OF AN X-RAY LITHOGRAPHY CELL: COMPARISON OF 200MM AND 300MM WAFERS", Proceedings of the 1999 Winter Simulation Conference, pp. 865-874
		Pierce, et al., "MODELING AND SIMULATION OF MATERIAL HANDLING FOR SEMICONDUCTOR WAFER FABRICATION", Proceedings of the 1994 Winter Simulation Conference, pp. 900-906
		Robinson, et al., "CAPACITY PLANNING FOR SEMICONDUCTOR WAFER FABRICATION WITH TIME CONSTRAINTS BETWEEN OPERATIONS", Proceedings of the 1999 Winter Simulaiton Conference, pp. 880-887

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.